

UNIVERSITY OF BRISTOL

Practice Paper

School of Computer Science

**First in-class test for the Degree of
Master of Science in Computer Science (conversion)**

**COMSM1302
Overview of Computer Architecture**

**TIME ALLOWED:
2 Hours**

Answers

Other Instructions

1. Make sure you carefully read any instructions on the question paper and answer booklet.
2. You must use the answer booklet to answer all questions.
3. No calculators may be used for this examination.
4. This is a closed-book examination; books, notes, or other resources are forbidden.
5. A reference sheet will be given out alongside the question paper.
6. Any of the question paper can be used for rough work, but only the answer booklet will be marked.

TURN OVER ONLY WHEN TOLD TO BEGIN WORK

Section 1 – Short-answer questions (50 marks total)

You do not need to justify your answers for any of the questions in this section, and you will not receive partial credit for showing your reasoning. Just write your answers down in the shortest form possible, e.g. “A” for multiple-choice questions, “true” for true/false questions, or “23” for numerical questions. If you do display working, circle or otherwise indicate your final answer, as if it cannot be identified then the question will not be marked.

Question 1 (4 marks)

Mark each of the following statements true or false.

- (a) $(A \wedge B) \vee (C)$ is in disjunctive normal form. (1 mark)

Solution: true (it is in disjunctive normal form)

- (b) $(B \vee \neg A) \wedge (C \vee A)$ is in disjunctive normal form. (1 mark)

Solution: false (it is in conjunctive normal form)

- (c) $\neg(A \vee B) \vee (\neg B \wedge C)$ is in disjunctive normal form. (1 mark)

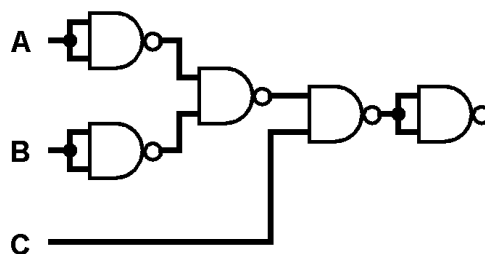
Solution: false (it is not in disjunctive normal form or conjunctive normal form)

- (d) $(C \wedge \neg A \wedge B) \vee (B \wedge \neg B)$ is in disjunctive normal form. (1 mark)

Solution: true (it is in disjunctive normal form)

Question 2 (4 marks)

Consider the below NAND circuit diagram.



The following Boolean expression is logically equivalent to the NAND circuit.

$$(A \text{ <OP1> } B) \text{ <OP2> } C$$

- (a) Which logical operator should replace <OP1>? (2 marks)

Solution: $\vee$ or OR

- (b) Which logical operator should replace <OP2>? (2 marks)

Solution: $\wedge$ or AND

Question 3 (5 marks)

Consider the Hack ALU specification.

- (a) What function is carried out, if the control bit **f** is set to 0? (1 mark)

Solution: Logical AND

- (b) What happens to input x , if the control bits zx and nx are both set to 1? (2 marks)

Solution: Sets it to -1 (as it sets it to 0, then negates it)

- (c) What will out compute, if the controls are set as $zx = 0$, $nx = 1$, $zy = 1$, $ny = 1$, $f = 0$, and $no = 1$? (2 marks)

Solution: $x (\neg(\neg x \wedge \neg 0) \equiv \neg(\neg x \wedge 1) \equiv \neg(\neg x) \equiv x$

Question 4 (5 marks)

Mark each of the following statements true or false.

- (a) A latch is level-triggered.

(1 mark)

Solution: true (as set out in week 3 video 2, this is the difference between latches and flip-flops - latches are level-triggered while flip-flops are edge-triggered)

- (b) It is faster to access data stored in RAM than in ROM.

(1 mark)

Solution: false (there's no intrinsic difference in access speeds between RAM and ROM - it depends on the exact types of memory used e.g. the EEPROM used in a flash drive is much slower than DDRRAM, which in turn is slower than a dedicated PROM programmed by blowing out transistors)

- (c) A Mealy machine requires more states than the equivalent Moore machine. (1 mark)

Solution: false (in fact any Moore machine can be re-implemented as a Mealy machine with the same number of states)

- (d) A demultiplexer with 2 select bits will select between 4 inputs.

(1 mark)

Solution: false (wrong way round - a demultiplexer with 2 select bits will select between 4 *outputs*)

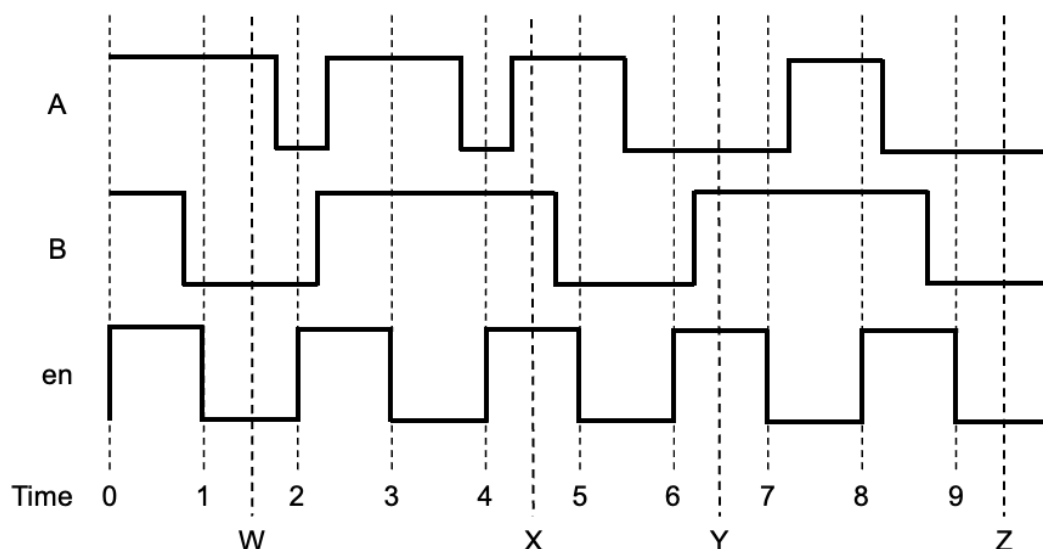
- (e) Given a low input, a one-shot outputs high for exactly one clock cycle.

(1 mark)

Solution: false (a one-shot normally activates given a high input, not a low input)

Question 5 (4 marks)

Consider the below negative edge-triggered D flip-flop waveform, and the corresponding outputs Q and Q'.



The flip-flop's D input is connected to the signal A XOR B, which updates immediately after the value of A or the value of B changes.

- (a) At time point W, what is the value of the flip-flop's output Q?

(1 mark)

Solution: 1 (at the last falling clock edge $A = 1$ and $B = 0$, so $A \text{ XOR } B = 1$ i.e. the value stored in the flip-flop and therefore output through Q)

- (b) At time point X, what is the value of the flip-flop's output Q? (1 mark)

Solution: 0 (at the last falling clock edge $A = 1$ and $B = 1$, so $A \text{ XOR } B = 0$ i.e. the value stored in the flip-flop and therefore output through Q)

- (c) At time point Y, what is the value of the flip-flop's output Q'? (1 mark)

Solution: 0 (at the last falling clock edge $A = 1$ and $B = 0$, so $A \text{ XOR } B = 1$ i.e. the value stored in the flip-flop and therefore its inverse, 0, is output through Q')

- (d) At time point Z, what is the value of the flip-flop's output Q'? (1 mark)

Solution: 1 (at the last falling clock edge $A = 0$ and $B = 0$, so $A \text{ XOR } B = 0$ i.e. the value stored in the flip-flop and therefore its inverse, 1, is output through Q')

Question 6 (4 marks)

Which of the following statements comparing memory is **false**?

- A. An SRAM chip has lower capacity than a DRAM chip of the same physical size.
- B. A flip-flop provides faster access speeds than an SRAM cell.
- C. An SDRAM cell is a type of DRAM cell, and has nothing to do with SRAM.
- D. A DRAM cell is more expensive to build than a flip-flop.

Solution: D

D is false, as flip-flops take around 12-30 transistors to build, whereas DRAM cells are built using only 1 transistor plus a capacitor, making them cheaper to build.

A is true, as SRAM cells take up more physical space as they use 4-6 transistors to build.

B is true, as a flip-flop's stored value is always immediately available on its Q output.

C is true, as mentioned in lecture 3.4.

Question 7 (6 marks)

Consider the 8-bit binary number 1001 0010.

- (a) What is its decimal value, if it uses unsigned representation? **(2 marks)**

Solution: 146 ($128 + 16 + 2 = 146$)

- (b) What is its decimal value, if it uses signed-magnitude representation? **(2 marks)**

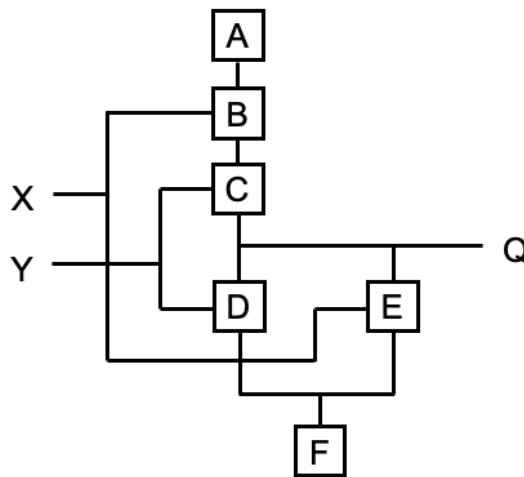
Solution: -18 ($16 + 2 = 18$, then the most significant bit is 1 so this becomes -18)

- (c) What is its decimal value, if it uses 2's complement representation? **(2 marks)**

Solution: -110 ($-128 + 16 + 2 = -110$)

Question 8 (6 marks)

Consider the below diagram of a NAND gate composed of transistors.



- (a) Which voltage is connected at the marked location A? **(1 mark)**

Solution: Vss or source or ground

- (b) Which type of MOS transistor is connected at the marked location B? **(1 mark)**

Solution: n-type or nMOS

- (c) Which type of MOS transistor is connected at the marked location C? **(1 mark)**

Solution: n-type or nMOS

- (d) Which type of MOS transistor is connected at the marked location D? **(1 mark)**

Solution: p-type or pMOS

- (e) Which type of MOS transistor is connected at the marked location E? **(1 mark)**

Solution: p-type or pMOS

- (f) Which voltage is connected at the marked location F? **(1 mark)**

Solution: Vdd or drain

Question 9 (6 marks)

For each of the following clock time periods, give the equivalent clock frequency, in hertz.

- (a) $25ms$ (2 marks)

Solution: 40Hz ($25ms = 0.025s$, frequency = $1/0.025 = 40/1 = 40Hz$)

- (b) $500\mu s$ (2 marks)

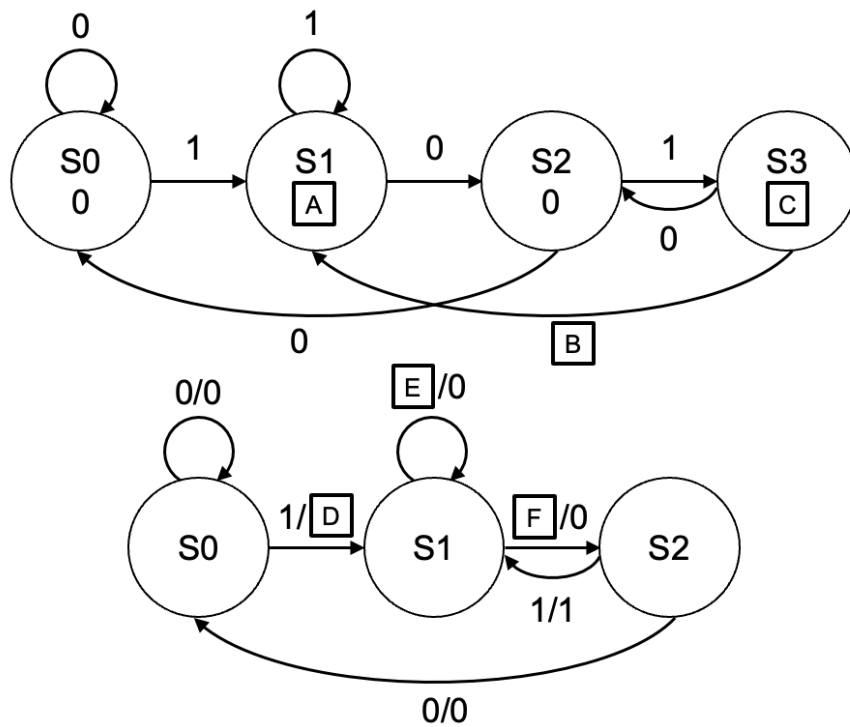
Solution: 2000Hz ($500\mu s = 0.0005s$, frequency = $1/0.0005 = 2/0.001 = 2000Hz$)

- (c) $4s$ (2 marks)

Solution: 0.25Hz ($4s = 4s$, frequency = $1/4 = 0.25Hz$)

Question 10 (6 marks)

Consider the below state transition diagrams, each representing the same finite state machine.



Solution: When turning the Mealy machine into a Moore machine, state S1 would have different outputs depending which transition was used to get there and so this is split on the Moore machine into S1 (for an output of 0) and S3 (for an output of 1).

- (a) Will the value at the marked location A be 0, 1, or impossible to determine? **(1 mark)**

Solution: 0 (the transition on the Mealy machine from S1 to itself outputs 0)

- (b) Will the value at the marked location B be 0, 1, or impossible to determine? **(1 mark)**

Solution: 1 (the other transition from S3 on the Moore machine has an input of 0)

- (c) Will the value at the marked location C be 0, 1, or impossible to determine? **(1 mark)**

Solution: 1 (the transition on the Mealy machine from S2 to S1 outputs 1)

- (d) Will the value at the marked location D be 0, 1, or impossible to determine? **(1 mark)**

Solution: 0 (S1 on the Moore machine outputs 0)

- (e) Will the value at the marked location E be 0, 1, or impossible to determine? **(1 mark)**

Solution: 1 (the transition on the Moore machine from S1 to itself has an input of 1)

- (f) Will the value at the marked location F be 0, 1, or impossible to determine? **(1 mark)**

Solution: 0 (the transition on the Moore machine from S1 to S2 has an input of 0)

Section 2 – Long-answer questions (50 marks total)

In this section, you should give the reasoning behind your answers unless otherwise specified. You will receive credit for partial answers or for incorrect answers with sensible reasoning.

Question 11 (10 marks)

Consider the below truth table.

A	B	C	Out
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

- (a) Write a Disjunctive Normal Form (DNF) Boolean expression for the truth table, where each term represents exactly one row of the truth table. (3 marks)

Solution: $(\neg A \wedge \neg B \wedge C) \vee (\neg A \wedge B \wedge C) \vee (A \wedge B \wedge C)$

- (b) i. Draw a Karnaugh map that represents the truth table with boxes around appropriate groups of 1s, such that it will give a DNF Boolean expression with as few terms and variables per term as possible. (4 marks)

C \ AB	00	01	11	10
0	0	0	0	0
1	1	1	1	0

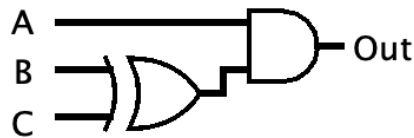
Solution:

- ii. Write a DNF Boolean expression that is given by your answer to part (b)(i). (3 marks)

Solution: $(\neg A \wedge C) \vee (B \wedge C)$

Question 12 (13 marks)

Consider the below logical circuit.



- (a) Write a Boolean expression that directly corresponds to the circuit, using a combination of $\wedge$, $\vee$, and $\neg$ operators only. **(3 marks)**

Solution: $A \wedge ((B \wedge \neg C) \vee (\neg B \wedge C))$

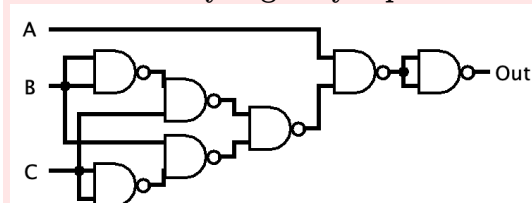
- (b) Draw a truth table for the circuit, which shows all possible input combinations and their corresponding output values. **(4 marks)**

Solution:

A	B	C	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

- (c) Draw a logically equivalent circuit, which only uses 2-input NAND gates. **(6 marks)**

Solution: Any logically equivalent circuit that only uses 2-input NAND gates e.g.:



Question 13 (7 marks)

Consider a **4-bit adder** constructed from four 1-bit full adders, with 4-bit inputs **X** and **Y**, and a 1-bit input **C_in**.

- (a) Write a Boolean expression for a **1-bit full adder's** output **C_out**. (3 marks)

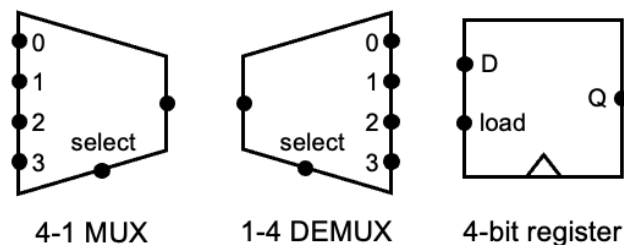
Solution: $(C_in \wedge B) \vee (A \wedge B) \vee (C_in \wedge A)$ or any logically equivalent expression

- (b) Explain how this arrangement can be modified to calculate **X - Y**, referring to specific inputs of each full adder. (4 marks)

Solution: Connect a constant 1 pin to the **C_in** of the full adder adding the LSB from each of **X** and **Y**. Negate all the bits of **Y** before they each reach the **B** inputs of the relevant full adder.

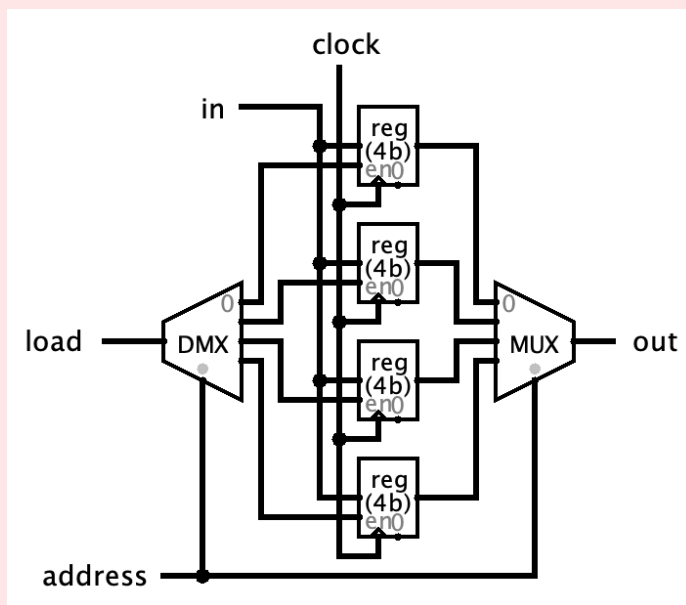
Question 14 (10 marks)

Draw a circuit for a **4-word RAM**, which takes a 4-bit input **in**, a 2-bit input **address**, a 1-bit input **load**, a 1-bit clock input, and produces a 4-bit output **out**. Only components shown below, as well as copies of them, are permitted.



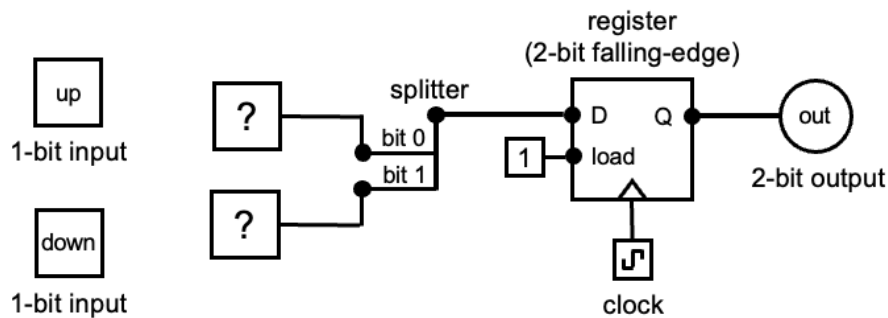
You may draw components in any orientation or style, as long as its inputs and outputs are unchanged. Label every component you use, along with its inputs and outputs.

Solution: Something that resembles the construction of the below image diagram.



Question 15 (10 marks)

A partial circuit is shown below, with 1-bit inputs **up** and **down**, and 2-bit output **out**. The boxes containing ? each represent a missing part of the circuit. Wires drawn with a thick line carry a 2-bit signal, while wires drawn with a thin line carry a 1-bit signal.



The inputs **up** and **down** will never be 1 at the same time, and on a falling clock edge:

- If the input **up** is 1, the value of **out** should increase by 1 e.g. if **out** was previously 00 then it should now be 01. However, if **out** was previously 11 then it should stay 11.
- If the input **down** is 1, the value of **out** should decrease by 1 e.g. if **out** was previously 11 then it should now be 10. However, if **out** was previously 00 then it should stay 00.

The circuit's signals are labelled as follows:

Variable	Meaning
up	the input up
down	the input down
A	MSB of the register's output Q
B	LSB of the register's output Q

- (a) Give a Boolean expression for the **bit0** input of the splitter. (5 marks)

Solution: $(A \wedge up) \vee (\neg B \wedge up) \vee (B \wedge \neg up \wedge \neg down) \vee (A \wedge \neg B \wedge down)$ or any logically equivalent expression

$\begin{matrix} \text{up/down} \\ \backslash AB \end{matrix}$	00	01	11	10
00	0	1	1	0
01	0	0	0	1
11	X	X	X	X
10	1	0	1	1

- (b) Give a Boolean expression for the **bit1** input of the splitter. (5 marks)

Solution: $(A \wedge B) \vee (A \wedge \neg \text{down}) \vee (B \wedge \text{up})$ or any logically equivalent expression

AB updown	00	01	11	10
00	0	0	1	1
01	0	0	1	0
11	X	X	X	X
10	0	1	1	1

END OF EXAMINATION

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