From flip-flops to registers COMSM1302 Overview of Computer Architecture

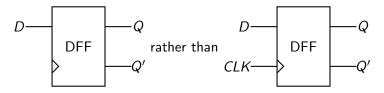
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Clocked circuits

Recall from last time our big idea: we drive all our timings with a *single* clock signal.



If an edge-triggered circuit is driven by this clock, we denote it by a triangle. To save space, since all circuits use the same clock, we often don't draw in the wire. So e.g. a D flip-flop is often drawn as:



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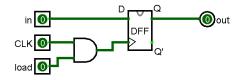


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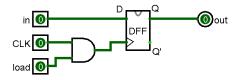
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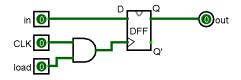


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On a rising clock edge, if *load* is high, *out* takes on the value of *in*. If *load* is low, *out* remains unchanged. How should we design this?



This design fails. Can you see why? Because here, *out* takes on the value of *in* on a rising edge of *load* \land *CLK*, not of *CLK*. So if e.g. *load* oscillates while CLK is high, *out* is unstable.

In general when working with flip-flops, it's a bad idea to mess with the clock signal — it's easy to introduce bugs like this. Instead...

1-bit registers: the correct way!

We use the outputs from one clock cycle to set the inputs for the next, using combinatorial logic. We want:

in	load	$\mathit{out}_{\mathrm{old}}$	$\mathit{out}_{\mathrm{new}}$
Х	0	0	0
Х	0	1	1
0	1	Х	0
1	1	Х	1

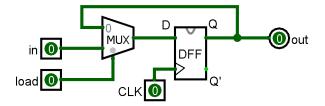
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Here as last video, X means "don't care". We could expand this out into a full truth table and use a K-map... or just notice that this is a multiplexer!



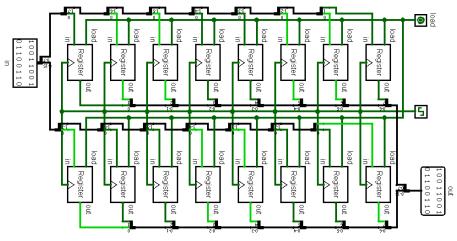
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It's simple to implement a 16-bit register, but it's a good excuse to show how buses and clocks work in Logisim.



[See video for a demonstration of assorted features in Logisim. The circuit is available for download in readable form from the unit page.]