Microarchitecture optimisation: Pipelining and caching COMSM1302 Overview of Computer Architecture

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Pipelining by analogy

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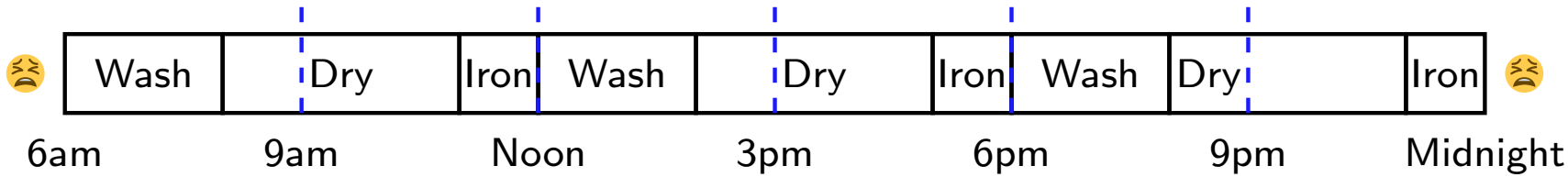

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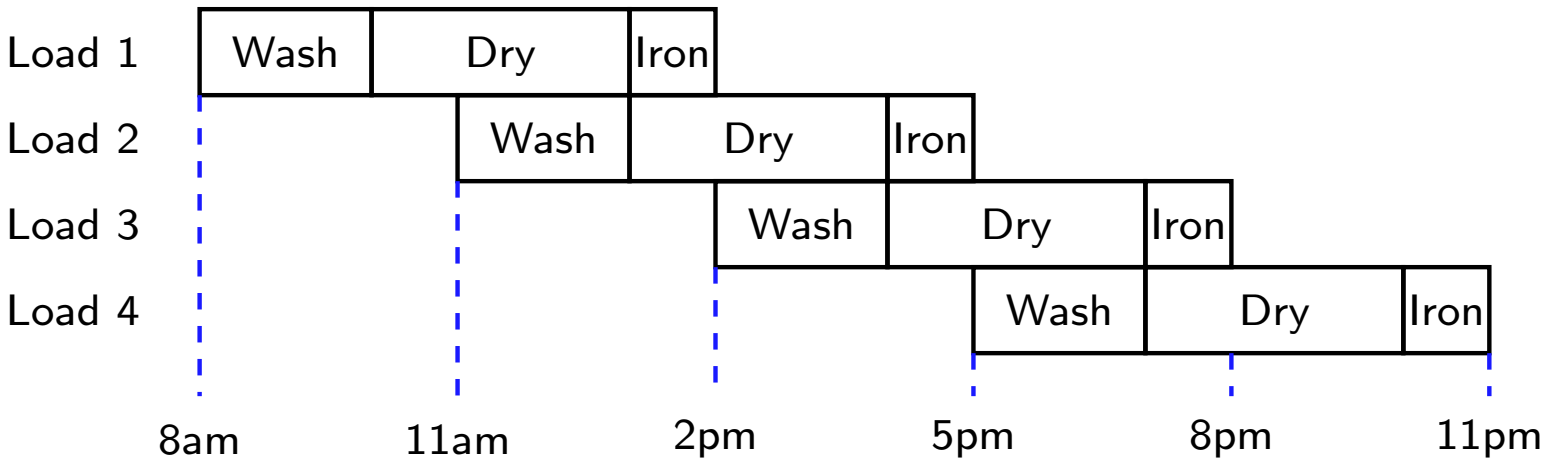

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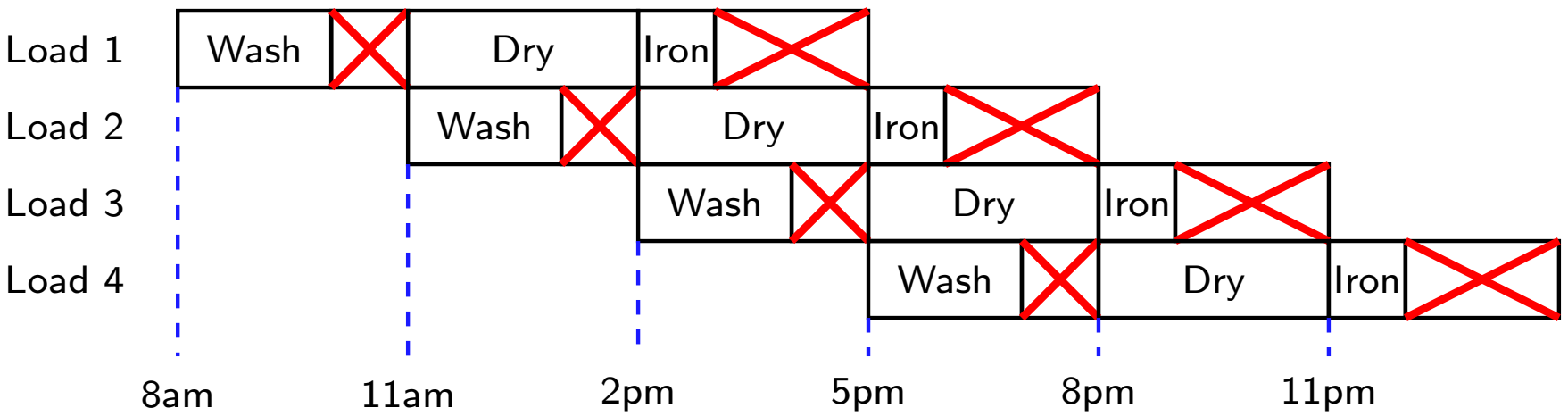

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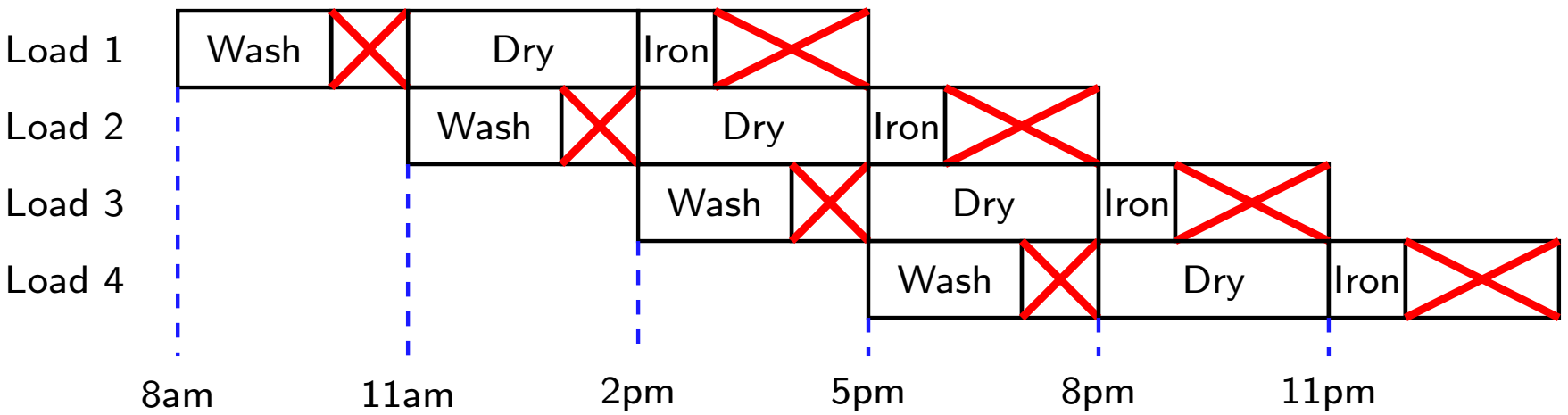

The moral: By parallelising where we can to avoid letting components sit idle, we can massively increase throughput! This is called **pipelining**.

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For C-instructions in Hack, we could divide the fetch-execute cycle into four stages (some of which would be skipped for A-instructions):

- **Fetch**: Fetch the next instruction from ROM[PC].
- **Decode**: Set the inputs for the ALU to the appropriate values.
- **Execute**: Set the outputs of the ALU to the appropriate values.
- **Writeback**: Write values to RAM and registers, update PC.

Each stage uses different hardware, so we can set the clock speed to the propagation delay of the slowest stage, rather than of the entire fetch-execute cycle!

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Modern CPUs have more complex pipelines than this, but the same principles hold and these four stages are still a good basic framework.

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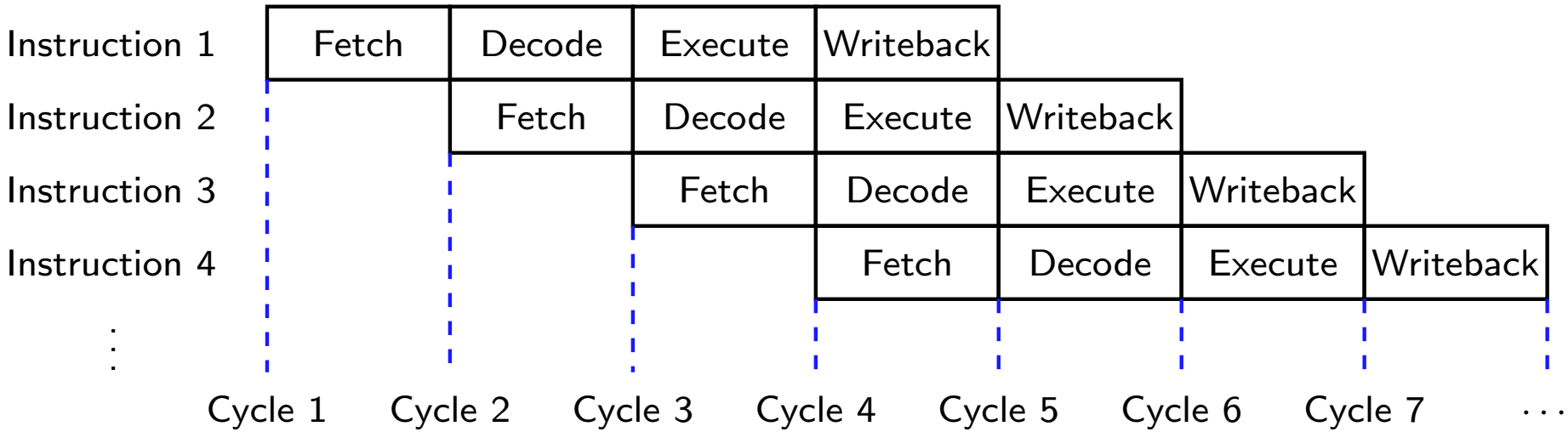
So our fetch-execute cycle would become:



What could go wrong?

The reality of pipelining: Stalls and hazards

- **Data hazards** arise when an instruction needs access to data modified by an earlier instruction that hasn't finished evaluating.
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Any of these hazards can lead to a **stall** (a.k.a. **bubble**), where the rest of the pipeline stops moving until the offending instruction completes.

Avoiding and mitigating stalls is a complex part of modern CPU design.

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With multiple cores, all these problems get much worse!

Source: Imgur (here)

Most benefits come from either the operating system dividing cores between applications, or from the developer writing explicitly parallel code.

Memory caching

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That's roughly 0.175ns per cycle.

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- A 16+GB address space means more complex electronics and therefore more propagation delay.
- 16+GB of SRAM would be prohibitively expensive, so we use DRAM.
- Physical distance from the chip! (Electricity moves at light speed, which is roughly 3×10^8m/s, so 3.33ns to move one metre...)

Modern CPUs address this with smaller, faster, closer **memory caches**.

How caching works

Modern CPUs use three caches: L1, L2, and L3. For Zen 4 (roughly):

Data location	Capacity	Cycles to access	Time to access
Registers	1.8KB/core[1]	1	0.175ns
L1 cache	64KB/core	4	0.7ns
L2 cache	1MB/core	14	2.45ns
L3 cache	4MB/core	50	8.75ns
DDR5 RAM	16–64GB	418	73ns
Fast SSD	0.5–4TB	140,000	25μs
Fast HDD	0.5–4TB	28,500,000	5ms

Instructions are loaded into the L1 cache in advance. Where possible, at conditional branches, we "look ahead" and load both possible options.

Otherwise, the most frequently used data (e.g. memory used for common variables) goes to the L1 cache, then L2, then L3, then main memory.

[1] This is for the 224 integer registers — there are a few hundred others as well.

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Minimising the number of accesses to main memory ("**cache misses**") is a very important part of both CPU design and code optimisation.

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Applications of architecture: Predication

Understanding pipelining tells us ifs and loops require branches, which create control hazards and are disproportionately slow.

But evaluating a logical expression to 0 or 1 doesn't create a control hazard. It might create a data hazard, but it's still faster overall. E.g.:

```
if (x <= 50) {
    y += 10;
} else {
    y = 3;
}
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becomes

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y = (y+10)*(x <= 50) + 3*(x > 50);
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This technique is called **predication** or **branchless programming**.

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As with inserting assembly fragments, it's *only* a good idea for code you already know is a performance bottleneck. Otherwise it's not worth the bugs, the time spent, or the loss of clarity and maintainability.

(Modern compilers are also smart, so you may do more harm than good!)

Applications of architecture: Loop unrolling

Loop unrolling is the practice of writing out several iterations of a simple loop by hand to minimise the number of branches. For example:

```c
// Copy the first [count] entries of [from] to [to].
int broke_array_copy(int from[], int to[], int count)
{
    for(int i=0; i<=count; i++)
        to[i] = from[i];
}
```

becomes

```c
// Copy the first [count] entries of [from] to [to].
int woke_array_copy(int from[], int to[], int count)
{
    while (count >= 8) {
        *to = *from;
        to += 1;
        from += 1;
        // Repeat these three lines 6 more times
        *to = *from;
        to += 1;
        from += 1;
        count -= 8;
    }
    while (count > 0) {
        *to = *from;
        to += 1;
        from += 1;
        count -= 1;
    }
}
```

Say $\texttt{count} = 500$. Then the left code will use $\texttt{count} + 1 = 501$ conditional branches. The right code will only use $(1 + \texttt{count}/8) + (1 + \texttt{count}\,\%8) = 68$. (We've also saved 500 addition operations by removing i.)

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```
// Copy the first [count] entries of [from] to [to].
int bespoke_array_copy(int from[], int to[], int count)
{
    register int n = (count + 7) / 8;
    switch (count % 8)
    {
        case 0:                 do {  *to++ = *from++;
        case 7:                       *to++ = *from++;
        case 6:                       *to++ = *from++;
        case 5:                       *to++ = *from++;
        case 4:                       *to++ = *from++;
        case 3:                       *to++ = *from++;
        case 2:                       *to++ = *from++;
        case 1:                       *to++ = *from++;
                                  } while (--n > 0);
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                                  } while (--n > 0);
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The code above is (a version of) **Duff's device**. Its creator, Tom Duff, said:

"Many people (even [Brian Kernighan]?) have said that the worst feature of C is that switches don't break automatically before each case label. This code forms some sort of argument in that debate, but I'm not sure whether it's for or against."